

## Analog Subsystem for the Internet Rack Monitor

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The analog section of the Fermilab Internet Rack Monitor (IRM) consists of two components; the analog interface IndustryPack module mounted on the MVME162 CPU card, and the offboard analog I/O board that mounts to the back panel of the IRM. Eight channels of D-A analog output and sixty four channels of analog input are provided.

Two circuit boards make up the analog section of the IRM; Figure 1 is the analog I/O board and Figure 2 the analog IP interface module. The IP module is the same circuit board that is used as the interface to the Digital I/O section, but with a different design for the Field Programmable Gate Array. Figure 3 gives the pinout for the for this FPGA. The digitizer, 64 channel of analog inputs and eight D-As are located on the I/O board. Rear panel analog I/O connector pinouts are given in Figure 6.

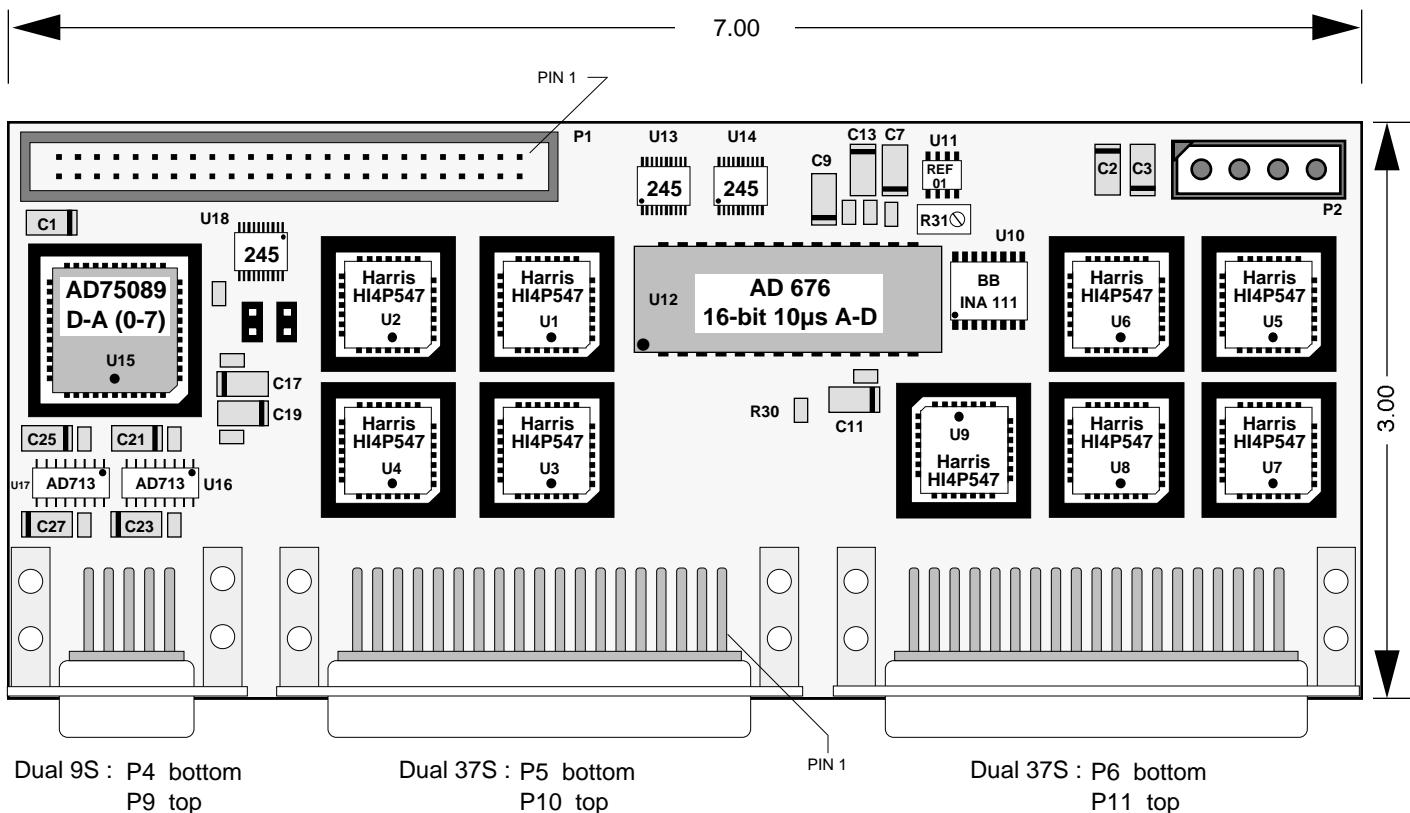
Operation of the multiplexer and digitizer are controlled by the IP module. All 64 analog channels are digitized sequentially at a rate of 12.5  $\mu$ s per channel. The full scan takes 800  $\mu$ sec to complete, and a new scan is triggered at 1 ms intervals. Data from the digitizer scans are stored sequentially in 64 Kbytes of memory located on the IP module. About 500 data sets fit in the memory, and when the memory is full, the pointer wraps around and begins overwriting the oldest data. RAM on the IP module is accessible as IP memory as well as being used by the hardware to store A-D readings. By operating the digitizer in the mode described here, so-called 'fast-time-plot' data is available at 1 ms sample intervals for all 64 analog input channels. This type of data is of interest for data acquisition from synchrotrons and storage rings.

The analog to digital converter is an Analog Devices 676; a 16-bit, 10  $\mu$ s cycle digitizer. In this application, successive channels are digitized at 12.5  $\mu$ s per channel. Harris 547 8-channel differential multiplexers select the input signals. These multiplexers have internal overvoltage protection of  $\pm 35V$ . The selected differential

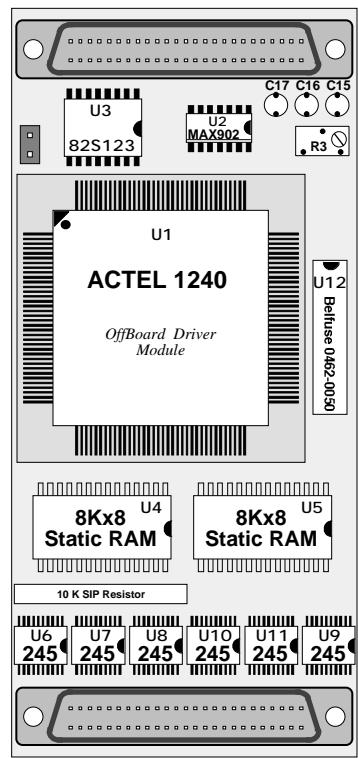
signal is input to a Burr Brown INA111 instrumentation amplifier that drives the digitizer input. A convert strobe to the digitizer isolates the converter section from the analog input for the duration of the digitize cycle. The next channel may be selected at that time to allow maximum settling time before the next digitize strobe.

Figure 4 shows the memory map for the IP Analog board. The 'Memory Address Pointer' register is the location in the 64 KByte memory where the next digitized result will be stored. Because the AD converts continuously, the pointer register is needed to select the most recent data from the 512 data sets stored in memory. Interrupts can be generated for end-of-scan condition or from an external source. Vectors for these are stored in the FPGA. AD-Calibrate is a location that may be written to cause the digitizer to execute its internal calibration sequence. ADBusy will be asserted high during calibrate and digitize cycles. Control register bits are given in figure 4. When the ADEnable bit is set high, the AD system begins digitizing and storing results in memory. For special applications, the AD scan repetition rate may need to be synchronized with external events. When the 'External Scan Enable' bit is set, an external trigger may be used to initiate a 64-channel scan.

Eight D-A channels are derived from an Analog Devices 75089 octal digital-to-analog converter. Because the output of the D-A has a  $\pm 5$  V range, a gain of two amplifier is used to provide a  $\pm 10V$  output range from the IRM.



## FIRM Analog Outboard



**Figure 2. Off Board Interface IP Module**

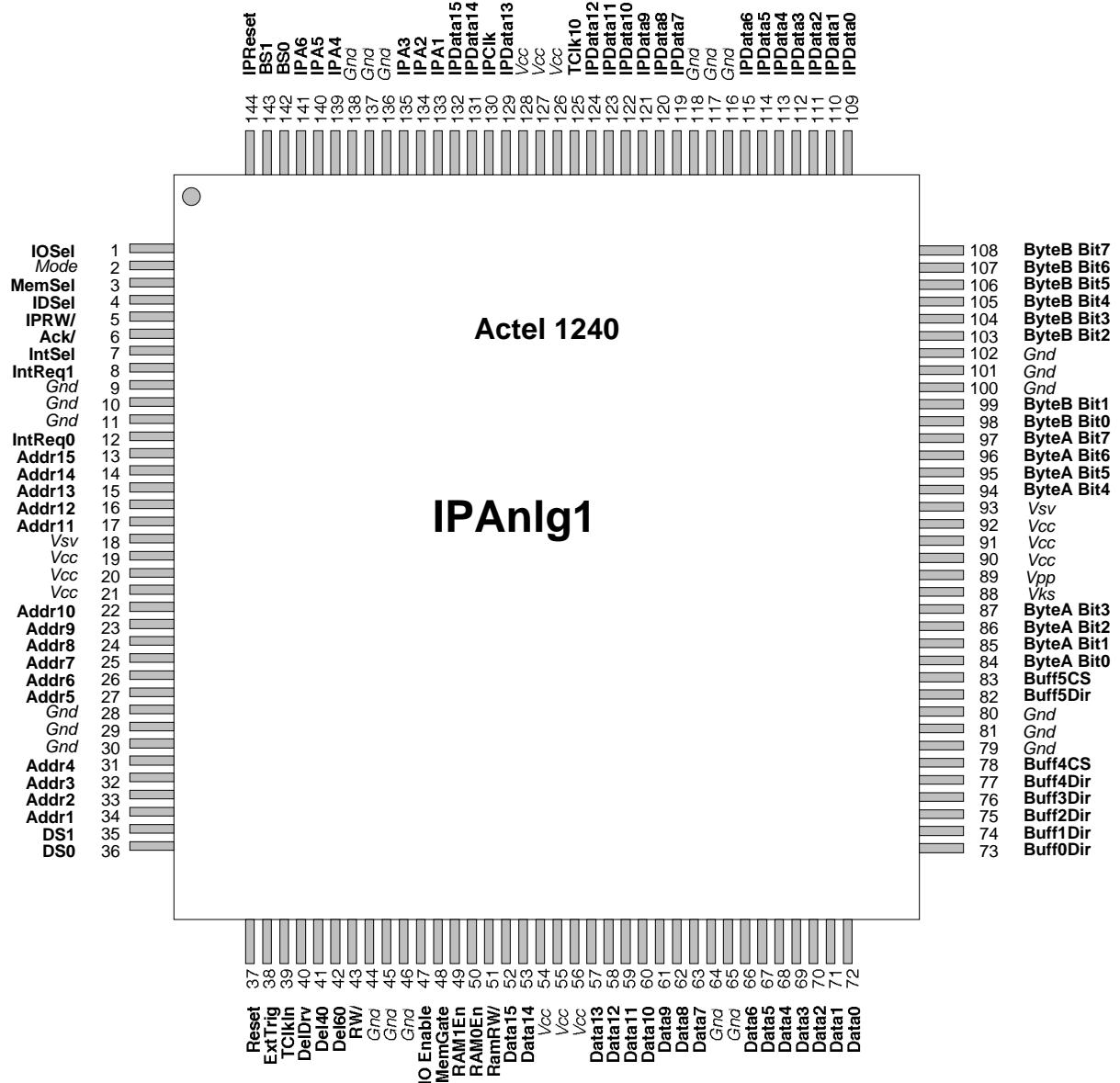
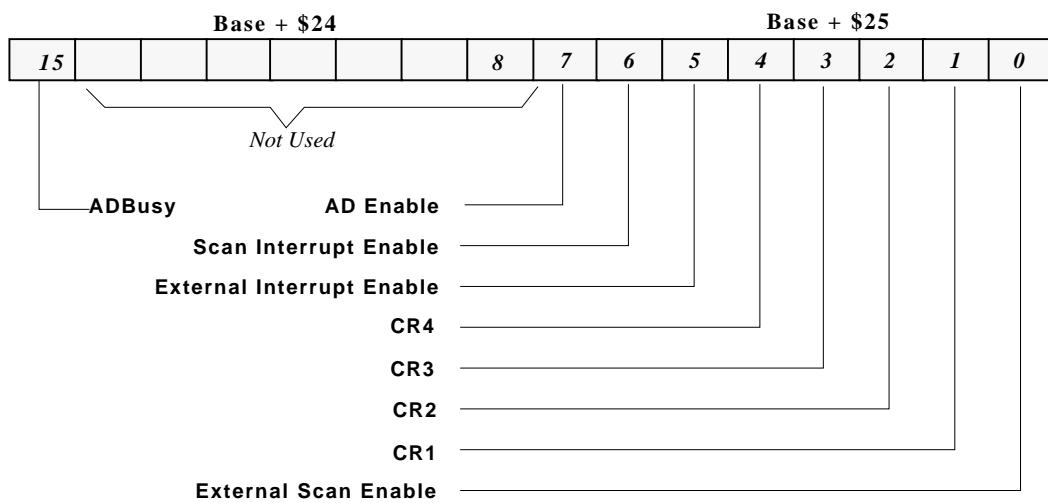


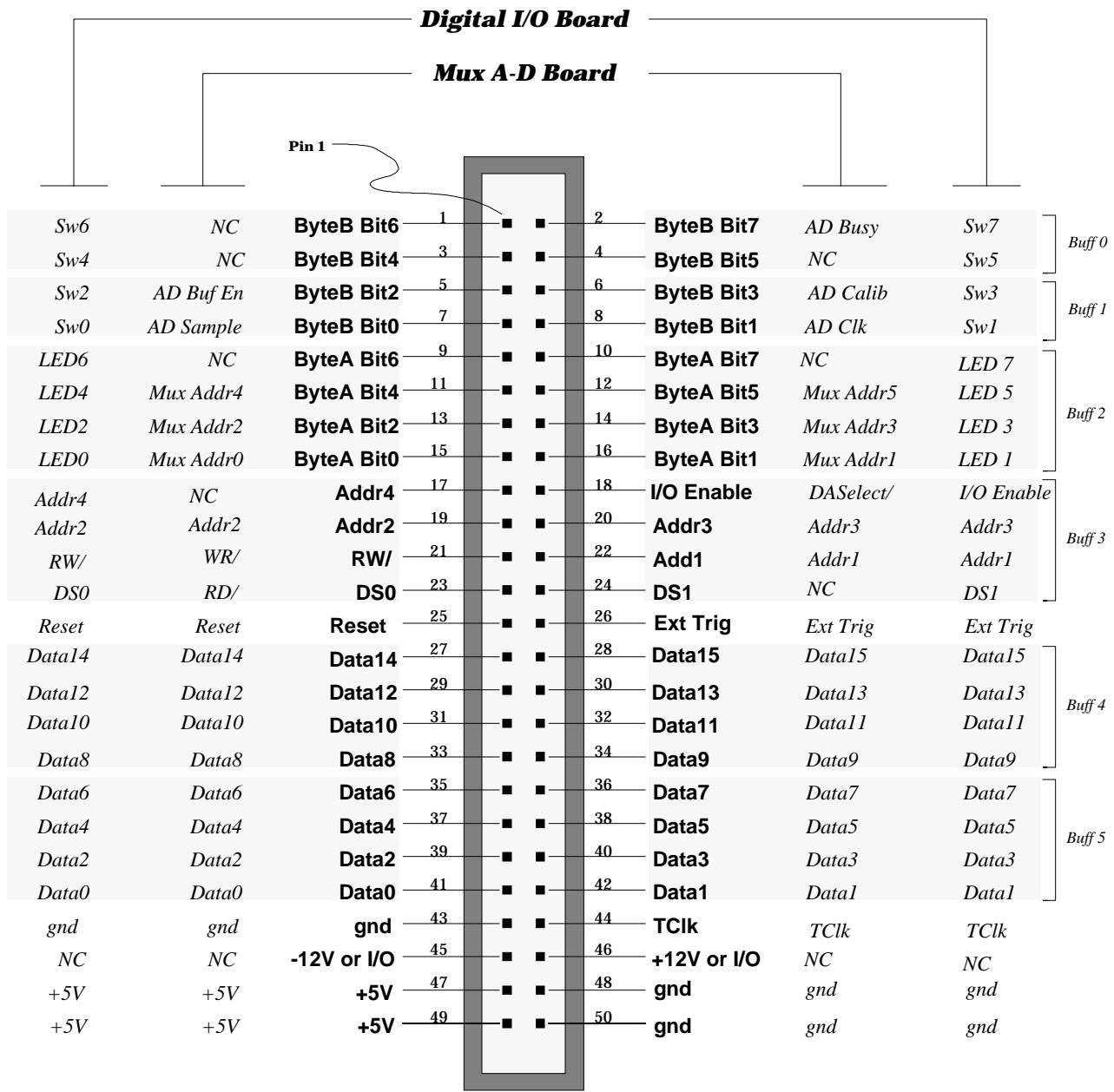
Figure 3. Offboard Interface Actel 1240 Pinout

Address				
Base + \$00	DA-0	DA-1	DA-2	DA-3
Base + \$08	DA-4	DA-5	DA-6	DA-7
Base + \$10	-	-	-	-
Base + \$18	-	-	-	-
Base + \$20	Mem Addr pointer	Int Vect0 • Int Vect1	ADBusy • Contr Reg	AD Calibrate
Base + \$28	-	-	-	-
Base + \$30	-	-	-	-
Base + \$38	-	-	-	-

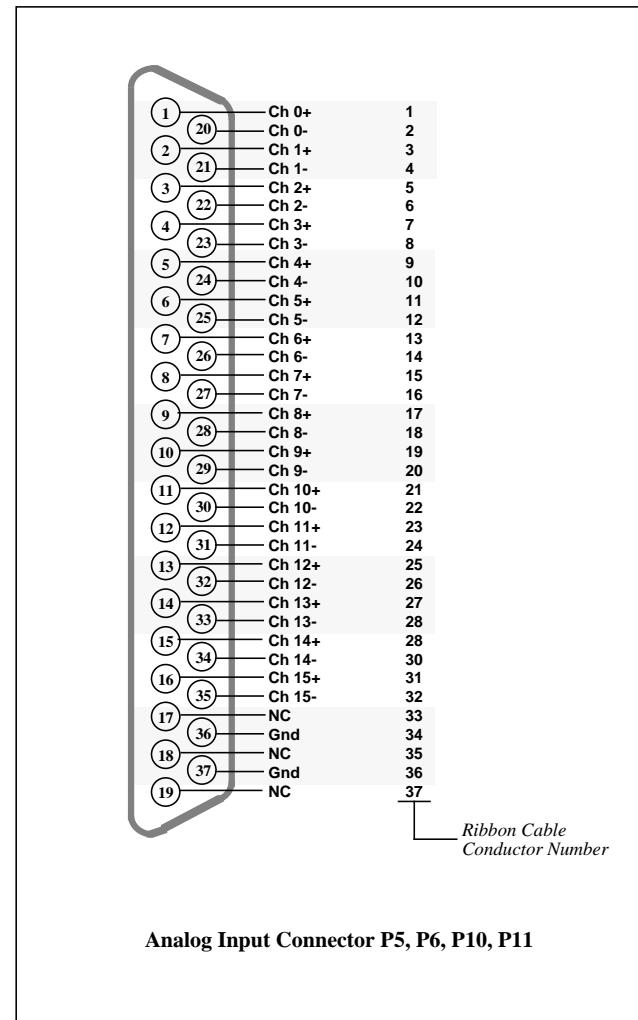
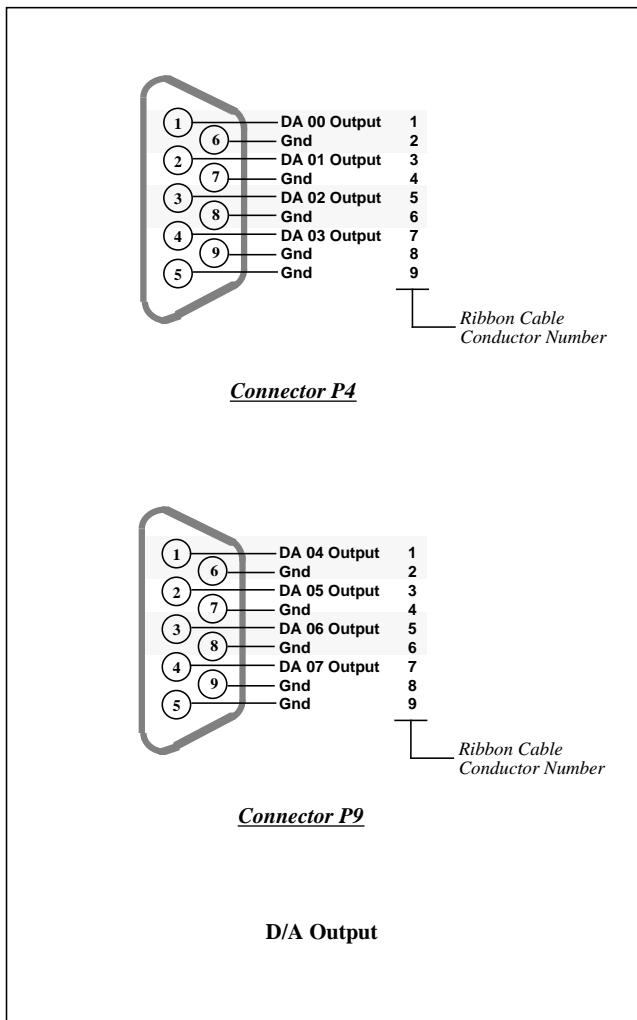
**Figure 4a. Memory Map for IPAnlg1 FPGA**



**Figure 4b. IPAnlg1 Control Register**



**Figure 5. I/O Interface Driver Connector Pinout**



**Figure 6. IRM Analog I/O Connector Pinouts**